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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,778	07/31/2003	Fong Shi	60000500.1012	7891

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,778	SHI, FONG	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,27-29 and 31-34* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The allowability of claims 18 and 33 are withdrawn because of the new references are found.

Claim Objections

2. Claims 1, 5, 15 and 17 are objected to because of the following informalities: a phrase "a Backside Interconnect" should be changed to "a backside interconnect". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 7, 10, 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by McKay (US. 5,945,734).

Regarding claim 1, McKay (Fig. 2) discloses a near-hermetic microwave semiconductor device comprising: a substrate 22; a MMIC 10 (column 2, lines 20-28) disposed on the substrate; a sealant 18 disposed on the MMIC 10; and a backside interconnect connecting the substrate 22 to the sealant-coated MMIC 10, including plated-through vias 16 disposed in the MMIC 10 extending between opposite faces of the MMIC 10, and tying to terminals 24 on the substrate.

Regarding claims 2 and 7, McKay's Fig. 2 further discloses that the substrate 22 is a PWB suitable for high frequency applications (column 3, lines 30-35), and a MMIC is a GaAs MMIC (column 3, lines 9-12).

Regarding claim 10, McKay's Fig. 2 further discloses that a solder attachment 26 along a periphery of the MMIC, to near-hermetically seal the MMIC to the substrate.

Regarding claims 12 and 14, McKay's Fig. 2 further discloses a conformal coating or a cover 28 disposed on the sealant 18.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-7, 9-14, 15-17, 27-29, and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinayman et al (US. 2003/0151133) in view of Maley (US. 6,249,136) and Chun et al (US. 6,710,542).

Regarding claims 1, 6, 13-15 and 34, Kinayman (Fig. 10) discloses a near hermetic microwave semiconductor device, comprising: a substrate; a MMIC 6 (par. [0046]) disposed on the substrate; a backside interconnect 42 electrically connecting the substrate to the MMIC 6, and typing to terminals (not labeled) on the substrate by the solder balls 41; and a cover 1 disposed over the MMIC 6 in a non-contacting manner.

Maley does not specifically disclose that the backside interconnect includes plated-through vias extending between opposite faces of the MMIC 6.

However, Maley (Figs. 6 and 7) teaches the forming of a flip-chip 102 having a backside interconnect including plated-through vias 112 extending between opposite faces of the chip 102. Accordingly, it would have been obvious to include the plated-through vias extending between opposite faces of Kinayman's MMIC 6 because such plated-through vias would provide the electrical signal connections to and from the circuitry on the top surface to the bottom surface of the MMIC, as taught by Maley (column 6, lines 20-23).

Neither Kinayman nor Maley disclose a sealant disposed on the MMIC (claim 1), and an interlayer dielectric disposed between the sealant and the MMIC (claims 6 and 15).

However, Chun (Fig. 2) teaches a near-hermetic device comprising a first sealant layer 22 disposed on the electronic package, and a first interlayer dielectric 21 of BCB (column 4, lines 9-21) disposed between the first sealant layer 22 and the electronic package. Accordingly, it would have been obvious to modify the semiconductor package of Kinayman by forming the sealant and the interlayer dielectric with the structure as set forth above because as taught by Chun, such sealant and interlayer dielectric structures would provide a sealing layer which prevents the moisture and oxygen from reaching the chip (column 4, lines 11-17).

Regarding claims 2-4, 27-29, and 31, Kinayman (Fig. 10) further discloses that the MMIC 6 is a GaAs MMIC, and the substrate is formed of a ceramic PWB (par.

[0003] and par. [0049]) suitable for high frequency applications, such as RF and millimeter-wave integrated circuit packaging (par. [0001]).

Regarding claims 9-11, 16 and 32, Kinayman's Fig. 10 further discloses that the backside interconnect of MMIC 6 connecting to a bottom ground plane 9 of the substrate (par. [0052]), and a solder attachment 41 along a periphery of the MMIC 6 to near-hermetically seal the MMIC 6 to the substrate. It would have been obvious to form the solder attachment 41 made of AuSn because AuSn is well-known solder material which has a low melting point.

Regarding claims 12, 17 and 33, Chun (Fig. 2) further teaches the forming of a second interlayer dielectric 21 and a second sealant layer 22 functioning as a conformal coating disposed on the first interlayer dielectric 21 and the first sealant layer 22 for more effectively preventing the moisture and oxygen from reaching the chip (column 4, lines 11-17).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zuo et al (US. 6,525,420) in view of Maley (US. 6,249,136) and Ross (US. 5,572,070).

Regarding claim 5, Zuo (Fig. 4) discloses a near-hermetic semiconductor device, comprising: a substrate 7; an integrated circuit 9 disposed on the substrate; a cover 20 disposed on the integrated circuit 9; and a backside interconnect 13 connecting the substrate to the integrated circuit 9, and tying to terminals on the substrate 7 (column 4, lines 15-24). The integrated circuit 9 of Zuo can be used as a MMIC depending upon the desired device application.

Zuo does not specifically disclose the backside interconnect includes plated-through vias extending between opposite faces of the integrated circuit 9.

However, Maley (Figs. 6 and 7) teaches the forming of a flip-chip 102 having a backside interconnect including plated-through vias 112 extending between opposite faces of the chip 102. Accordingly, it would have been obvious to include the plated-through vias extending between opposite faces of Zuo's integrated circuit 9 because such plated-through vias would provide the electrical signal connections to and from the circuitry on the top surface to the bottom surface of the chip, as taught by Maley (column 6, lines 20-23).

Neither Zuo nor Maley disclose a silicon carbide sealant disposed on the integrated circuit.

However, Zuo further discloses that a sealant for heat transfer may be positioned between the top surface of the integrated circuit 9 and the cover 20 to thermally couple them together (column 4, lines 34-38). And Ross (Fig. 3) teaches the forming of a sealant 20 for heat transfer positioned between the top surface of the integrated circuit 13 and the cover 17 to thermally couple them together, the sealant 20 is made of silicon carbide (column 6, lines 1-4 and lines 61-65). Accordingly, it would have been obvious to form Zuo's sealant with silicon carbide because silicon carbide is also a heat conductive material used for heat transfer, as taught by Ross (column 6, lines 1-4 and lines 61-65).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zuo et al, Maley, and Ross as applied to claim 5 above, and further in view of Kunihisa (US. 2002/0153616).

Claim 8 is read by the combination of Zuo, Maley and Kunihisa. Zuo does not disclose that the solder bumps can be used for the solder balls 13.

However, Kunihisa (Fig. 2) teaches the forming of a microwave semiconductor device having a MMIC 212 connected to a substrate by solder bump 213. Accordingly, it would have been obvious to substitute the solder balls 13 with the solder bumps because they are both well known in the art for providing the electrical contacts between the chip and the substrate in the flip-chip technology.

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kinayman et al, Maley and Chun et al as applied to claim 17 above, and further in view of Kunihisa et al (US. 2002/0153616).

Claim 18 is read by the combination of Kinayman, Maley and Chun. Kinayman further discloses that the coating is a low dielectric having a dielectric constant suitable for operating at an operation frequency within 2 GHZ and about 10 GHZ (see Figs. 11 and 12). Kinayman does not disclose that the solder bumps can be used for the solder balls 41.

However, Kunihisa (Fig. 2) teaches the forming of a microwave semiconductor device having a MMIC 212 connected to a substrate by the solder bumps 213. Accordingly, it would have been obvious to substitute the solder balls 41 with the solder

bumps because they are both well known in the art for providing the electrical contacts between the chip and the substrate in the flip-chip technology.

Allowable Subject Matter

10. Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

See the reasons of record.

Response to Arguments

11. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. However, because of the new issues presented in the amended claims, the new references are cited and the new final rejection is applied.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
June 10, 2005

PHAT X. CAO
PRIMARY EXAMINER